AMENDMENTS TO THE **SUBSTITUTE** SPECIFICATION:

Please replace the paragraph beginning at page 20, line 11 of the substitute specification with the following:

Fig. 3 illustrates a stacked gate structure as an example of the nonvolatile memory cell. The nonvolatile memory cell MC shown in the drawing is formed with a channel area between a source area 40 connected to source line (a second data line) SL, a drain area 41 connected to the source line SL, and a drain area 42 connected to bit line (a first data line) BL. Drain areas 41 and 42 can include an n+ region ("n+"). The stacked gate structure can also include an n- region ("n-"), a p+ region ("p+"), a p- region ("p-"), and a p substrate ("p-Sub"). A floating gate electrode 43 is formed via a gate insulating film over the channel area. A control gate electrode 44 is formed via an oxide film thereover. The floating gate electrode 43 is made by a polysilicon layer. The control gate electrode 44 is made by a polysilicon wire and becomes part of word line WL.

Please replace the paragraph beginning at page 23, line 10 of the substitute specification with the following:

Fig.5 illustrates a detail of a hierarchal bit line structure of the memory mat performing differential sense. In the example of Fig.5, the sense amplifiers ("sense amps")

SA(L) and SA(R) have ~~has~~ a differential amplification form performing differential input to a pair of memory arrays adjacent to each other on the upper and lower sides of the drawing. Sense amplifiers SA(L) and SA(R) also receive an input signal CBL and operate in accordance with control signals SPC(L), SPC(R), SEN(L) and SEN(R). One of a pair of differential inputs is a read signal from the bit line BL selected by one of the memory arrays and the other input is a reference input. The differential sense contributes to a faster read operation. The read main bit line GBLr is provided with a main amp MA so that the read operation is much faster. A differential amp is used as the main amp MA. One of a pair of main bit lines GBLr (L), GBLr (R) is a read signal input and the other is a reference input. The main amp MA is differentiated so that the read operation is much faster. The differential main amp MA is employed so that Fig.5 is different from Fig.4 in that the sense amp SA is provided for 32 bit lines BL as a unit and 64 sense amps are totally provided. Both are similar in that the write processing unit to the nonvolatile memory is 1024 bits and the external input and output unit is 32 bits.

Please replace the paragraph beginning at page 24, line 4 of the substitute specification with the following:

The main amp MA has transfer gate ~~TG~~ TRG switch-controlled by equalize signal MEQ and making the corresponding pair of read main bit lines GBLr (L), GBLr (R) conductive, static latch LAT connected to the corresponding pair of read main bit lines GBLr (L), GBLr (R) and actively and inactively controlled by amp enable signal MEN, and output inverter INV whose input terminal is connected to the input/output node on one side of the static latch LAT and whose output terminal is connected to the bus driver BDRV.

Please replace the paragraph beginning at page 24, line 13 of the substitute specification with the following:

Fig.6 shows an example of the sense amp SA (L) for differential sense. In the drawing, p channel type MOS transistors whose gate electrodes are indicated by small circles are discriminated from n channel type MOS transistors. It has differential input MOS transistors Q5, Q6 connected respectively to output signal line CBL (T) of one of memory arrays and to output signal line CBL (B) of the other memory array. These are connected to a latch circuit in a static latch form by MOS transistors Q1 to Q4. The MOS transistors Q1, Q4 are provided respectively with initializing MOS transistors Q7, Q8 in parallel to be connected to the source voltage. The common source of the

MOS transistors Q5, Q6 is connected via a power switch MOS transistor Q11 to the ground voltage Vss of the circuit. The gates of transistors Q7 and Q11 are connected to sense amplifier control signal SEN(L). Sense amplifier control signal SEN(R) is connected to corresponding transistor gates in sense amplifier SA(R) (not shown in Fig. 6). One of a pair of storage nodes of the latch circuit of the MOS transistors Q1 to Q4 is connected to the gate of a MOS transistor Q9 of the output inverter. The other is inverted and connected to the gate of a MOS transistor Q10 of the output inverter. The common drain of the MOS transistors Q9, Q10 constructing the output inverter is connected to the corresponding read main bit line GBLr. The numeral Q12 denotes an equalize MOS transistor of the CBL (T) and CBL (B). The numerals Q13, Q14 denote precharge MOS transistors. The gates of transistors Q12, Q13 and Q14 are connected to sense amplifier control signal SPC(L). Sense amplifier control signal SPC(R) is connected to corresponding transistor gates in sense amplifier SA(R) (not shown in Fig. 6). The numeral Q15 denotes a comparison current MOS transistor. The numerals Q16, Q17 denote transfer MOS transistors controlled by signals CCS(T) and CCS(B) selectively making the comparison current MOS transistor Q15 conductive to the signal lines CBL (T) and CBL (B). The

comparison current MOS transistor Q15 flows an electric current of half of an electric current flowing to the memory cell MC in the on state by a gate bias voltage CCB (Ion = Imen/2).

Please replace the paragraph beginning at page 26, line 15 of the substitute specification with the following:

When an address signal is changed at time t0, the selection state of the column decoder is changed in synchronization with it to start selection of the word line. During this, SPC (L) is brought to the low level to perform the precharge and equalize operations of the sense amp SA (L). The precharge and equalize operations of the sense amp SA (R) on the reference side remain disabled. The comparison current selection switches Q16, Q17 are brought into the off state at the precharge and equalize operations of the sense amp SA (L). The signal lines CBL (B) and CBL (T) are charged from the low level to the high level. When the precharge and equalize operations of the sense amp SA (L) are terminated, the comparison current selection switch Q17 on the non-sense side is turned on. On the signal line CBL (T) side, the level is changed according to the threshold voltage of the memory cell. On the signal line CBL (B) side, the level is changed according to the reference current flowed to the

Q15. Until the level change is increased to some degree, the sense amp SA (L) is inactive. During this, the main amp MA is equalized and the read main bit lines GBLr (R), GBLr (L) are brought to the intermediate level. When the sense amp SA (L) is activated at time t2, a difference voltage of the signal lines CBL (T) and CBL(B) is differentiated and amplified to amplify the read main bit lines GBLr (R), GBLr (L). The main amp MA is started up at time t3 to further amplify the read main bit lines GBLr (R), GBLr (L), thereby deciding the output OUT. In Fig. 7, signals SPC(L) <READ>, SPC(R) <REFERENCE>, SEN(L) <READ>, and SEN(R) <REFERENCE> are control signals to a sense amp, signals CCS <COMPARISON CURRENT SELECTION>, CCS(T), CBL(B) <REFERENCE>, and CBL(T) <READ> are input signals to a sense amp, and signals GBLr(R) <REFERENCE> and GBLr(L) <READ> are output signals of a sense amp.

Please replace the paragraph beginning at page 27, line 14 of the substitute specification with the following:

Fig. 8 shows another detail of the hierarchal bit line structure of the memory mat performing differential sense and having the differential amps SA(L) and SA(R). In a structure in which the sense amp and column selector circuit are connected between the memory arrays, it is assumed that

a high voltage is applied to the bit line BL at write or erase. In the operation speed of the sense amp and the column selector circuit, it is desirable that the transistor constructing the circuits is not a high-voltage MOS transistor. In this case, as shown in Fig.8, a disconnect circuit 50 connected and disconnected by the high-voltage MOS transistor may be provided between the memory array and the column selector circuit. Not only in the case of constructing the sense amp and the column selector circuit by the high-voltage MOS transistor, but also in a circuit structure in which a high voltage of write and erase is not applied to the bit line as in the split gate structure, the disconnect circuit 50 is unnecessary. Sense amplifiers SA(L) and SA(R) operate in accordance with control signals SPC(L), SPC(R), SEN(L) and SEN(R).

Please replace the paragraph beginning at page 31, line 21 of the substitute specification with the following:

Fig. 12 illustrates operation timings of write processing and read processing to memory arrays different from each other. In Fig. 12, signal WL(WRITE) is the word line in a write operation, signal GBLw(WRITE) is the write bit line (reference Fig. 2), signal WL(READ) is the word line in a read operation, and signal GBLw(READ) is the read

main bit line. Fig.13 illustrates an application example of the flash memory of Fig.11. The memory arrays of part of the memory mat 20 are a storage area (rewrite sequence area) 74 storing a rewrite sequence program of the flash memory and the remaining memory arrays are a storage area (user memory area) 75 which can be freely rewritten by the user. As explained based on Fig.11, the hierarchal bit line structure realizing the hierarchal sense method is disconnected from the write bit line structure to perform write and read in parallel in the same memory cycle. While reading and executing the rewrite sequence program, the memory of the user area can be rewritten. As illustrated in Fig.14, a command for rewrite control is fetched directly from the rewrite sequence area 74 to perform rewrite to the user memory area 75 based on it (S1 of Fig. 15). Fig.15 illustrates a rewrite control procedure. The CPU 3 fetches the command for rewrite control directly from the rewrite sequence area 74 to set control data to a rewrite control register of the control circuit 32 based on it (S2). For write, the CPU 3 transfers write data to the flash memory 9 (S3). The flash memory 9 selects a predetermined area of the user memory area 75 by an address signal. For write, a write voltage is applied, and for erase, an erase voltage is applied (S4).

Please replace the paragraph beginning at page 33, line 19 of the substitute specification with the following:

Figs.16 to 18 are diagrams of assistance in explaining a first pipeline access form assuming the address mapping. Fig.16 is a schematic block diagram of the flash memory when realizing the first pipeline access form. In Fig. 16, SA(L) and SA(R) refer to sense amps. Fig.17 is a logic circuit diagram of the decoder. Fig.18 is a timing chart of a pipeline read operation. In Figs. 16-18, WLa, WLb, WLc, and WLd are word lines; SPCa, SPCb, SPCc, SPCd, SENa, SENb, SENc, and SENd are sense amp control lines.

Please replace the paragraph beginning at page 35, line 13 of the substitute specification with the following:

Figs._19 to 21 are diagrams of assistance in explaining a second pipeline access form assuming the address mapping. Fig._19 is a schematic block diagram of a flash memory when realizing the second pipeline access form. Fig._20 is a logic circuit diagram of the decoder. In Fig. 20, RDECab is a decoder. Fig._21 is a timing chart of a pipeline read operation. In the flash memory realizing the second pipeline access form, the sense amp SA must employ the structure of Fig._22 in place of Fig._6.

Please replace the paragraph beginning at page 35, line 21 of the substitute specification with the following:

In Fig._19, for each of the hierarchies A, B, C and D, suffixes a, b, c or d is given to the word line WL, the precharge signal SPC, the sense amp enable signal SEN and the read main bit line drive signal GBLrDRV, which are representatively shown; that is, GBLrDRVa, GBLrDRVb, GBLrDRVc, and GBLrDRVd are read main bit line drive signals; WLa, WLb, WLc, and WLd are word lines; and SPCa, SPCb, SPCc, SPCd, SENa, SENb, SENc, and SENd are sense amp control lines for the respective hierarchies A, B, C and D. The decoder shown in Fig._19 is a generic term for the row decoder RDEC and the column decoder CDEC. SA(L) and SA(R) refer to sense amps.

Please replace the paragraph beginning at page 37, line 2 of the substitute specification with the following:

The structure of the sense amp SA for performing such pipeline access is as illustrated in Fig._22. In order to separately control the timings of the sense and output operations, in the structure of Fig._6, the output operation of the MOS transistors Q9, Q10 is enabled after the read main bit line drive signal GBLrDRV is activated, and OR gates 90, 91 and an inverter 92 are added. In Fig. 22, SA(L)

is a sense amp; SPC(L) and SEN(L) are control signals of a sense amp; and CCS(T), CBL(T), CBL(B), CCB, and CCS(B) are input signals of a sense amp.

Please replace the paragraph beginning at page 39, line 13 of the substitute specification with the following:

Fig. 25 schematically shows the flash memory when realizing the read data conflict prevention. The drawing illustrates memory arrays for two hierarchies A, B. The verify main bit lines GBLv are provided corresponding to the read main bit lines GBLr. MAr for read and MAv for verify as the main amps are provided to right and left areas UT. Their outputs are selected by selector SEL. The inputs of the main amp MAr for read are connected to the read main bit lines GBLr of the corresponding right and left areas UT in which one of them is on the sense side and the other is on the reference side. The inputs of the main amp MAv for verify are connected to the main bit lines GBLv for verify of the corresponding right and left areas UT in which one of them is on the sense side and the other is on the reference side. The verify read data is transmitted via the data bus to the CPU, not shown, for comparison. Other constructions are the same as the constructions explained in Figs. 4 and 5. In

Fig. 25, SA(L) is a sense amp and GBLv [VERIFY GBL] and GBLr [READ GBL] are output signals of a sense amp.

Please replace the paragraph beginning at page 40, line 24 of the substitute specification with the following:

Fig._27 schematically shows another flash memory when realizing the read data conflict prevention. It is different from Fig._25 in that the main amp MA is arranged for the read main bit line GBLr and verify comparator CMP is arranged for the verify main bit line GBLv. The verify comparator CMP compares the write data supplied from the data bus with the data read from the verify main bit line GBLv to decide whether the write operation is completed or not. In Fig. 27, SA(L) is a sense amp and GBLv [VERIFY GBL] and GBLr [READ GBL] are output signals of a sense amp.

Please replace the paragraph beginning at page 41, line 6 of the substitute specification with the following:

Fig._28 shows an operation timing chart of Fig._27. Fig._28 shows an example in which in Fig._27, the hierarchy A performs a read operation and the hierarchy B performs a verify read operation as the first step of a write operation. The timing chart of Fig._28 shows an example in which timing in which the read GBL drive signal GBLrDRVa is

enabled in the hierarchy A and the sense amp SA (L) of the hierarchy outputs read data to the read main bit line GBLr is the same as timing (1-CYCLE ACCES) of a clock signal (1-CYCLE) in which the verify GBL drive signal GBLvDRVb is enabled in the hierarchy B and the sense amp SA (L) of the hierarchy outputs read data to the verify main bit line GBLv. In this case, a signal amplified by the main amp MA connected to the read main bit line GBLr is outputted to the data bus. In parallel with this, the verify comparator CMP connected to the verify main bit line GBLv compares the write data with the data read from the verify main bit line GLBv. In the write data circuit, not shown, including the verify comparator CMP, the write operation is continued when the comparison result indicates that the write operation is not completed. The write is terminated to the memory cell to be written connected to the verify main bit line GBLv when the comparison result indicates that the write operation is completed. In Fig._27, the write data is inputted directly from the data bus to the input of the verify comparator CMP which has an output signal CMP (VERIFY COMPARATOR). Actually, it should be understood that the write data is inputted via the write data latch and other write circuits, not shown.

Please replace the paragraph beginning at page 42, line 8 of the substitute specification with the following:

Fig._29 illustrates a detail of the sense amp SA used in the embodiment shown in Figs._25 to 28. The sense amp shown in the drawing has a selector circuit part deciding, by the read GBL drive signal GBLrDRV and the verify GBL drive signal GBLvDRV, to which of an output driver connected to the read main bit line GBLr and having the transistors Q9, Q10 and an output driver connected to the verify main bit line GBLv and having the transistors Q20, Q21 an output signal is supplied. The selector part has gate circuits 90 to 95. The structure of Fig._29 is different from of that of Fig._22 in that the output driver having the transistors Q20, Q21 and the selection logic having the gate circuits 90 to 95 are added. The sense amp SA is thus constructed to amplify and output a signal read from the memory cell to any one of the read main bit line GBLr and the verify main bit line GBLv in one amp circuit. In Fig. 29, signals CBL(T), CBL(B), CCB, CCS(B), CCS(T), and CCS(B) are input signals of a sense amp; signal SPC(L) is a control signal of a sense amp; and GBLr [READ GBL] and GBLv [VERIFY GBL] are output signals of a sense amp.